UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,104	09/17/2003	Toshinari Takayanagi	004-9196	3693

22120 7590 03/21/2005

ZAGORIN O'BRIEN GRAHAM LLP
7600B N. CAPITAL OF TEXAS HWY.
SUITE 350
AUSTIN, TX 78731

EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,104	TAKAYANAGI, TOSHINARI	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 0704+1104
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-58 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 11/01/2004

Information Disclosure Statement (IDS) filed on 07/12/2004.

3. Information disclosed and list on PTO 1449 was considered.

Specification

2. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Regarding claim 32, lines 1, should be deleted a "wherein".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Eleyan et al. (U. S. Patent No. 6,762,961).

Regarding claims 24-55, Eleyan et al. disclose a circuit comprising:

first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices (Column 2, lines 16-35); and

a preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device (Column 1, lines 15-55). More specifically, Eleyan et al. disclose wherein the first and second matched devices together comprise a cross-coupled pair of transistors within a sensing circuit of a semiconductor memory (Figure 2), and wherein the cross-coupled pair of transistors comprise PMOS transistors (Figure 2), and wherein the preconditioning circuit comprises means for applying a substantially uniform bias history across both first and

second matched devices (Column 2, lines 45-48), and wherein the preconditioning circuit comprises means for subjecting each of the matched devices to substantially equal time durations of a predetermined bias condition known to promote the shift in the characteristic (Column 1, lines 45-55), and wherein the matched devices comprise field effect transistors; and the predetermined bias condition includes a negative gate-to-source voltage (Figure 2, ABSTRACT), and wherein the preconditioning circuit is arranged to subject the matched devices to substantially equal time durations of a first bias condition corresponding to one data state as a second bias condition corresponding to another data state opposite the one data state (Column 2, lines 49-67), and wherein said one data state and said another data state are conveyed serially on a test data bus (Column 3, lines 1-19), and wherein the preconditioning circuit is arranged to subject both matched devices simultaneously to the predetermined bias condition (Column 3, lines 1-30), and wherein the preconditioning circuit is configured to be enabled during a burn-in operation (column 3, lines 19-30), and wherein the at least one characteristic susceptible to an accumulated data-dependent mismatch results, at least in part, from an effect that disparately affects one of the pair of matched devices as compared with the other, the disparate effect based on a skew in a history of values read out from associated memory elements (ABSTRACT), and wherein the disparate effect is associated with negative bias temperature instability, and wherein the disparate effect involves a monotonic change in the characteristic based on disparate voltage bias histories of the matched devices, and wherein the characteristic is mobility (Column 1, lines 46-55, Column 2, lines 49-67).

Regarding claims 56-57, Eleyan et al. disclose a computer readable encoding of a semiconductor integrated circuit design , the computer readable encoding comprising: one or more media encoding a representation of a memory circuit that includes plural pairs of bit lines, memory cells coupled to respective ones of the bit line pairs; the one or more media further encoding a representation of a sense amplifier circuit coupled to one or more respective ones of the bit line pairs for sensing data stored in associated memory elements, said sense amplifier circuit including first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices; and the one or more media further encoding a representation of a preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device (Figure 1), and wherein each of the one or more media are selected from the set of a disk, tape or other magnetic, optical, semiconductor or electronic storage medium and a network, wireline, wireless or other communications medium, and combination with one or more respective media readers therefor, wherein the one or more media and respective media readers, when combined, are exercisable to supply an information stream suitable to at least partially define one or more process steps for fabrication of semiconductor integrated circuits in accordance with the encoded design (Column 8, lines 58-67, Column 9, lines 1-8).

Regarding claims 1-23, the apparatus discussed above would perform the claim method 1-23.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER